Code No: P21CST03

HALL TICKET NUMBER

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### PACE INSTITUTE OF TECHNOLOGY & SCIENCES::ONGOLE
### (AUTONOMOUS)
### II B.TECH I SEMESTER END SUPPLEMENTARY EXAMINATIONS, MARCH/APRIL - 2023
### COMPUTER ORGANIZATION
### (Common to CSE, CSIT Branches)

Time: 3 hours                                             Max. Marks: 70

Answer all the questions from each UNIT (5X14=70M)

| Q.No. | | Questions | Marks | CO | KL |
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| | | **UNIT-I** | | | |
| 1. | a) | Draw and explain Block Diagram of Digital Computers. | [7M] | 1 | 2 |
| | b) | Evaluate the following arithmetic statement using zero, one, two and three address instructions. Use the conventional symbols and instructions. X = (A+B) * (C+D). | [7M] | 1 | 3 |
| | | OR | | | |
| 2. | a) | Give the list of Memory Reference Instruction. Explain any THREE of it. | [7M] | 1 | 1 |
| | b) | Explain about Stack Organization | [7M] | 1 | 2 |
| | | **UNIT-II** | | | |
| 3. | a) | Explain about Arithmetic Micro operations | [7M] | 2 | 2 |
| | b) | Give list of Basic computer register with their Size and Range? | [7M] | 2 | 1 |
| | | OR | | | |
| 4. | a) | Draw and explain a common bus system for four registers. | [7M] | 2 | 2 |
| | b) | Explain about Address sequencing | [7M] | 2 | 2 |
| | | **UNIT-III** | | | |
| 5. | a) | Discuss how addition and subtraction of signed magnitude numbers can be done? | [7M] | 3 | 2 |
| | b) | Explain BCD subtraction operation with an example | [7M] | 3 | 2 |
| | | OR | | | |
| 6. | a) | Explain in detail with neat sketch Booth Multiplication Algorithm | [7M] | 3 | 2 |
| | b) | Draw the flowchart for Floating point Arithmetic operation | [7M] | 3 | 1 |
| | | **UNIT-IV** | | | |
| 7. | | How many characters per second can be transmitted over a 1200 baud line in each of the following modes? <br> a) Synchronous serial transmission <br> b) Asynchronous serial transmission with two stop bits. <br> c) Asynchronous serial transmission with one-stop bits | [10M] | 4 | 2 |
| | | OR | | | |
| 8. | a) | Differentiate cycle stealing and Burst transfers of DMA. | [7M] | 4 | 3 |
| | b) | Explain about Cache Memory | [7M] | 4 | 2 |
| | | **UNIT-V** | | | |
| 9. | a) | Explain about Cache Coherence | [7M] | 5 | 2 |
| | b) | Explain about Pipelining. | [7M] | 5 | 2 |
| | | OR | | | |
| 10. | a) | Explain about Vector Processing | [7M] | 5 | 2 |
| | b) | Explain about RISC Pipeline | [7M] | 5 | 2 |

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